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PTO/SB/21 (07-06)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/893,340
Filing Date	June 26, 2001
First Named Inventor	Kang, Sien G.
Art Unit	2813
Examiner Name	Jack S.J. Chen
Attorney Docket Number	018419-008320US

Total Number of Pages in This Submission

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) (please identify below):

Appellants' Brief Under 37 CFR §41.37 and Declaration of Sien G. Kang (in triplicate)

Return Postcard

Remarks The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Townsend and Townsend and Crew LLP		
Signature			
Printed name	Kent J. Tobin		
Date	November 3, 2006	Reg. No.	39,496

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Signature	Sharyl Brown		
Typed or printed name	Sharyl Brown	Date	November 3, 2006

Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 500

Complete if Known	
Application Number	09/893,340
Filing Date	June 26, 2001
First Named Inventor	Kang, Sien G.
Examiner Name	Jack S.J. Chen
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METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 20-1430 Deposit Account Name: Townsend and Townsend and Crew LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims _____ -20 or HP = _____ x _____ = Fee Paid ($) _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims _____ -3 or HP = _____ x _____ = Fee Paid ($) _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims: Fee ($) _____ Fee Paid ($) _____

3. APPLICATION SIZE FEE

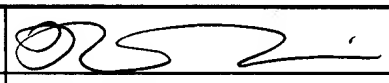
If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets _____ - 100 = _____ / 50 = _____ (round **up** to a whole number) x Fee ($) _____ = Fee Paid ($) _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Filing a brief in support of an appeal	500

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 39,496	Telephone 650-326-2400
Name (Print/Type)	Kent J. Tobin		Date November 3, 2006

PATENT
Attorney Docket No. 018419-008320US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No. 2640
SIEN G. KANG et al.	Examiner: Jack S.J. Chen
Application No.: 09/893,340	Technology Center/Art Unit: 2813
Filed: June 26, 2001	APPELLANTS' BRIEF UNDER 37 CFR §41.37
For: SURFACE FINISHING OF SOI SUBSTRATES USING AN EPI PROCESS	

Mail Stop Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Further to the Notice of Appeal mailed on September 12, 2006 for the above-referenced application, Appellants submit this Brief on Appeal.

1. REAL PARTY IN INTEREST

The real party in interest for the above-identified application is SILICON GENESIS CORPORATION ("SiGen"), having its principal place of business at 61 Daggett Drive, San Jose, California 95134. The instant application claims priority as a continuation of U.S. Nonprovisional Patent Application No. 09/399,985. Assignment of the parent application to SiGen is recorded in the U.S. Patent and Trademark Office on February 7, 2000 at Reel 010594/Frame 0778.

2. RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences related to the present appeal.

3. STATUS OF CLAIMS

Claims 1-28 are canceled.

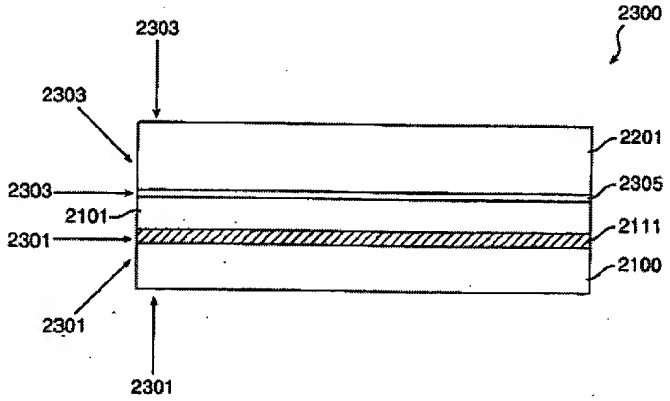
Claims 29-45 are pending and subject to this appeal. Claims 29-45 were rejected under 35 U.S.C. § 103(a) based on the grounds set forth in the Final Office Action mailed on May 15, 2006.

4. STATUS OF AMENDMENTS

All amendments to the claims have been entered. In accordance with 37 C.F.R. § 1.192(c)(9), a copy of the claims involved in the appeal are contained in the Appendix attached hereto.

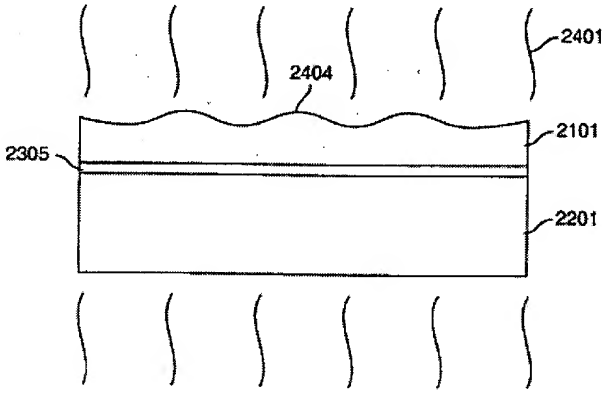
5. SUMMARY OF CLAIMED SUBJECT MATTER

Embodiments in accordance with the present invention relate to methods for reducing surface roughness of cleaved films. An embodiment of the present invention shown and described in connection with Figure 3 (reproduced below), describes forming a silicon-on-insulator (SOI) substrate, wherein two wafers are bonded together and then cleaved apart in a different location:



> After bonding the wafers into a sandwiched structure 2300, as shown in FIG. 3, the method includes a controlled cleaving action to remove the substrate material to provide a thin film of substrate material 2101 overlying an insulator 2305 the target silicon wafer 2201. The controlled-cleaving occurs by way of selective energy placement or positioning or targeting 2301, 2303 of energy sources onto the donor and/or target wafers. (Page 8, lines 1-6)

As illustrated in Figure 4 (reproduced below) of the instant specification:



the detached surface of the film of silicon material 2101 is often rough and needs finishing:

> to smooth or treat surface 2404, the substrate is subjected to thermal treatment 2401 in a hydrogen bearing environment. Additionally, the substrate is also subjected to an etchant including a halogen bearing compound such as HCl, HBr, HI, HF, and others. (Emphasis added; page 11, lines 4-8).

As a result of this treatment, roughness may be reduced by at least about eighty percent. (See page 3, lines 12-14, Abstract, and Figures 6-7).

Thus in accordance with embodiments of the present invention, the cleaved surface (of silicon material 2101 of Figures 3 and 4) is subjected to the following processes at the same time: (1) thermal treatment and (2) etching, thereby reducing roughness by at least about eighty percent. Pending independent claims 29 and 42 recite such embodiments:

> 29. A dry method for finishing SOI substrates, said method comprising:
> providing an SOI substrate comprising a cleaved surface, said cleaved surface having a first surface roughness value;
> performing a hydrogen treatment to increase a concentration of hydrogen of said cleaved surface; and
> performing an etchant and thermal treatment after the hydrogen treatment, the etchant and thermal treatment comprising:

increasing a temperature of an environment associated with said cleaved surface to greater than about 1,000° Celsius; and

contacting said cleaved surface with a hydrogen bearing environment at least when said temperature of said environment is greater than about 1,000° Celsius to reduce said first surface roughness value by at least about eighty percent to a second surface roughness value, said hydrogen bearing environment including at least an HCl gas and a hydrogen gas;

whereupon the cleaved surface having the second roughness value is substantially planarized.

* * *

42. A dry method for finishing SOI wafers, said method comprising:

providing an SOI wafer comprising a main surface that has been cleaved, said cleaved main surface having a first surface roughness value;

performing a hydrogen treatment to increase a hydrogen concentration of said cleaved main surface; and

performing an etchant and thermal treatment after the hydrogen treatment, the etchant and thermal treatment comprising:

increasing a temperature of an environment associated with said cleaved main surface to greater than about 1,000° Celsius; and

contacting said cleaved main surface with a hydrogen bearing environment at least when said temperature of said environment is greater than about 1,000° Celsius to reduce said first surface roughness value by at least about eighty percent to a second surface roughness value, said hydrogen bearing environment including at least an HCl gas and a hydrogen gas;

wherein the main surface is substantially planarized in its entirety to the second roughness value, the planarized main surface providing a surface whereon a plurality of devices are later defined.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 29, 31-38, and 43-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,251,754 to Ohshima et al. ("the Ohshima Patent"), in view of U.S. Patent No. 5,141,878 to Benton et al. ("the Benton Patent"), and Moriceau et al., "Hydrogen annealing treatment used to obtain high quality SOI surfaces", IEEE International SOI Conference, October 1998, pp. 37-38 ("the Moriceau Article").

B. Claims 40-42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Ohshima Patent in combination with the Benton Patent and the Moriceau Article, further in combination with Applicant's Admitted Prior Art (APA).

C. Claim 30 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the Ohshima Patent in combination with the Benton Patent and the Moriceau Article, and further in combination with Tate et al., "Defect Reduction of Bonded SOI Wafers by Post Anneal Process", Proceedings of 1998 IEEE International SOI Conference, Oct. 1998, pp. 141-142 ("the Tate Article").

D. Claim 39 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the Ohshima Patent in combination with the Benton Patent and the Moriceau Article, and further in combination with Published European Patent Application No. 0 553 852 A2 to Sato et al. ("the Sato Application").

7. ARGUMENT

A. Claims 29, 31-38, and 43-45 are not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over the Ohshima Patent in view of the Benton Patent and the Moriceau Article

Claims 29, 31-38, and 43-45 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Ohshima Patent in view of the Benton Patent the Moriceau Article.

As a threshold matter, it is noted that in order to establish a prima facie case of obviousness:

> there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. (MPEP 2143).

The teaching or suggestion to make the claimed combination must be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488 (Fed.Cir. 1991).

Here, the references being relied upon by the Examiner contain absolutely no teaching or even suggestion that would motivate their combination. Specifically, claims 29, 31-38, and 43-45 relate to formation of silicon-on-insulator (SOI) semiconductor substrates.

Applicants do not dispute that two of the references relied upon by the Examiner (the Ohshima Patent and the Moriceau Article) do relate to the field of substrate manufacturing. However, the Benton Patent - the third reference relied upon by the Examiner - does not bear any relation to the field of manufacturing SOI substrates.

Specifically, the Benton Patent describes fabrication of a particular type of electronic device on a substrate that has already been provided. In particular, the Benton Patent teaches creation of a photodiode structure that is monolithically integrated with other active electronic devices in the same semiconductor substrate. There is absolutely no teaching in the Benton Patent regarding manufacture of that substrate material, which in any event is specified as being a silicon substrate, not the silicon-on-insulator (SOI) substrate recited in the pending claims.

And while the Benton Patent does describe exposing a silicon surface to etching conditions, that surface is not the detached SOI surface of the Ohshima Patent. Rather, in the Benton Patent side walls and a bottom of a tub already created in a single crystal substrate, are etched locally in preparation for epitaxial growth of silicon in the tub to form a P/N junction:

> the p-n junction is formed by epitaxially growing thin, doped layers of silicon on the peripheral surfaces. As preliminary steps, the entrenched wafers can be subjected to a combined high temperature pre-bake and HCl--H_2 gas etch to reduce native oxide films and to further smooth the bottom and side walls of the tub. A five minute pre-bake and etch at 1025°C using 0.9 l/m of HCl and 40 l/m of H_2 is exemplary. (Emphasis added; col. 2, lines 46-53)

This passage comprises the entire disclosure of the Benton Patent regarding treatment under etching conditions. The Benton Patent includes no additional information that would reasonably lead one of ordinary skill in the art to perform such etching treatment globally upon the entire detached surface of the SOI substrate of the Ohshima patent. For example, the Benton patent fails to provide any ranges, or even numerical values, of changes in surface roughness of tub bottom or side walls that can be achieved utilizing the HCl--H_2 exposure. In view of the Benton Patent's omission of such information, it is difficult to understand how one of ordinary skill in the art would reasonably have been motivated to look to combine the Benton Patent with the Ohshima Patent.

Attached in the Evidence Appendix of this Appeal Brief is the signed declaration of inventor Sien Kang. Mr. Kang's declaration emphasizes that one of ordinary skill in the instant art of substrate manufacturing, would not have been motivated to turn to the different art of chip manufacturing, in order to duplicate the invention.

In his declaration, Mr. Kang emphasizes the separate nature of the substrate and device manufacturing disciplines, including the fundamental differences in their objectives and the

techniques relied upon. Specifically, claims 29, 31-38, and 43-45 relate to formation of silicon-on-insulator (SOI) semiconductor substrates. Such SOI substrates are typically fabricated by an independent manufacturer dedicated to this task, under specialized conditions and utilizing particular techniques and tools. For example, the starting materials for a SOI substrate manufacturing process typically include multi-layered wafer or substrates, including but not limited to silicon-on-silicon, silicon-on-oxide, and silicon-on-nitride, and silicon-on-quartz. Fabrication of a SOI substrate from these multi-layer materials typically involves a process of ten or fewer steps, which must be carried out under conditions that ensure global uniformity over the entire wafer surface. Examples of major manufacturers of SOI substrates include but are not limited to Soitec, MEMC, Walker Siltronic, and SEH.

Once formed, the SOI semiconductor substrate is then typically sold to members of a different industry group that are responsible for fabricating active electronic devices on the substrate, and then dicing the substrate into individual chips. The process for fabricating the active electronic devices typically involves a flow of more than fifty, and often more than a hundred, consecutive steps formed under precisely monitored conditions and affecting local areas of the substrate.

Examples of major chip manufacturers include but are not limited to Intel, Advanced Micro Devices, IBM, and others Few of these chip manufacturers also create the substrates that are the starting materials for the semiconductor chips.

Based upon the above arguments and the attached declaration, it is clear that art relied upon by the Examiner fails to provide any suggestion to motivate its combination in order to reject the pending claims.

Of course, consideration of the instant application provides ample suggestion to perform etching treatment to a cleaved surface of an SOI substrate. However, it is emphasized that the Manual of Patent Examining Procedure (MPEP) strongly cautions against relying upon Applicants' own disclosure in order to provide motivation to combine references:

> [t]he tendency to resort to "hindsight" based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art. (Emphasis added; MPEP 2142).

This strict prohibition against the use of hindsight, coupled with the lack of any apparent motivation in the Benton patent for its combination with the Ohshima patent or Moriceau Article, renders improper any conclusion of the obviousness of claims 29, 31-38, and 43-45 based upon those references.

B. Claims 40-42 are not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over the Ohshima Patent in view of the Benton Patent and the Moriceau Article, and further in view of Admitted Prior Art

Neither the Ohshima Patent nor the Moriceau Article (both relating to fabrication of a substrate), provide any motivation for their combination with the Benton Patent (relating to formation of a device in a substrate). The only possible motivation for combining these references arises out of Applicants' own teachings, which describe in detail the desirability of globally planarizing a cleaved surface of a substrate by performing etchant and thermal treatment after hydrogen treatment.

Such impermissible use of hindsight reasoning by the Examiner is only confirmed by the additional rejection of claims 40-42. Specifically, claims 40-42 recite fabrication of devices in a substrate. In order to reject these claims, the Examiner has found it necessary to combine the existing references with teachings from Applicants' own specification. Such unabashed reliance upon Applicants' own teachings to provide the critical nexus between fabrication of a substrate (as taught by the Ohshima Patent and Moriceau Article) and fabrication of devices in a substrate (as taught by the Benton Patent), amply evidences the complete failure of the references relied upon by the Examiner to provide this critical required element of the obviousness analysis.

The MPEP and caselaw cited therein strictly prohibit the use of hindsight reasoning to establish a prima facie case of obviousness. Here, the Examiner has signally failed to demonstrate any teaching or even suggestion that would motivate one of skill in the art to combine the references being relied upon to reject claims 40-42. The Examiner's use of hindsight reasoning to provide this absent motivation is not permissible, and no prima facie case of the obviousness of claims 40-42 has legitimately been established.

C. Claim 30 is not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over the Ohshima Patent in view of the Benton Patent and the Moriceau Article and further in view of the Tate Article

Claim 30 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the Ohshima Patent in combination with the Benton Patent and the Moriceau Article, and further in combination with the Tate Article.

Claim 30 depends from independent claim 29 discussed above, and recites as follows:

> 30. The method of claim 29 wherein the increasing the temperature is provided at a rate of about 10 Degrees Celsius per second and greater.

As discussed in detail above, the Ohshima Patent and the Moriceau Article references signally fail to provide any motivation that would lead one of ordinary skill in the art to combine them with the Benton Patent. Further combination of the Tate Article does nothing to cure this lack of motivation.

Specifically, like the Ohshima Patent and the Moriceau Article, the Tate Article describes SOI substrate technology, and in particular analyzes densities of defects observed in bonded SOI wafers. The Tate Article contains no teaching, or even suggestion, regarding fabrication of semiconductor devices, that would lead one of ordinary skill in the art to combine it with the Benton Patent. Because of this lack of any suggestion to combine reference teachings, it is respectfully asserted that claim 30 cannot be considered obvious in view of the combination of references relied upon by the Examiner.

D. Claim 39 is not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over the Ohshima Patent in view of the Benton Patent and the Moriceau Article and further in view of the Sato Application

Claim 39 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the Ohshima Patent in combination with the Benton Patent and the Moriceau Article, and further in combination with the Sato Application.

Claim 39 depends from independent claim 29 discussed above, and recites as follows:

> 39. The method of claim 29 wherein the environment is maintained at a pressure of about 1 atmosphere.

As discussed in detail above, the Ohshima Patent and the Moriceau Article references signally fail to provide any motivation that would motivate one of ordinary skill in the art to combine them with the Benton Patent. Further combination of the Sato Application does nothing to cure this lack of motivation. Specifically, like the Ohshima Patent and the Moriceau Article, the Sato Patent describes SOI substrate technology, and in particular heat-treating a substrate in a reducing atmosphere. The Sato Article contains no teaching or even suggestion regarding fabrication of semiconductor devices, that would motivate one of ordinary skill in the art to combine this reference with the Benton Patent. Because of this lack of any suggestion to combine reference teachings, it is respectfully asserted that claim 39 cannot be considered obvious in view of the combination of references relied upon by the Examiner.

8. CONCLUSION

For these reasons, it is respectfully submitted that the rejection should be reversed.

Respectfully submitted,

Kent J. Tobin
Reg. No. 39,496

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
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60879110 v1

9. CLAIMS APPENDIX

1-28. (Canceled)

29. (Previously Presented) A dry method for finishing SOI substrates, said method comprising:

providing an SOI substrate comprising a cleaved surface, said cleaved surface having a first surface roughness value;

performing a hydrogen treatment to increase a concentration of hydrogen of said cleaved surface; and

performing an etchant and thermal treatment after the hydrogen treatment, the etchant and thermal treatment comprising:

increasing a temperature of an environment associated with said cleaved surface to greater than about 1,000° Celsius; and

contacting said cleaved surface with a hydrogen bearing environment at least when said temperature of said environment is greater than about 1,000° Celsius to reduce said first surface roughness value by at least about eighty percent to a second surface roughness value, said hydrogen bearing environment including at least an HCl gas and a hydrogen gas;

whereupon the cleaved surface having the second roughness value is substantially planarized.

30. (Previously Presented) The method of claim 29 wherein the increasing the temperature is provided at a rate of about 10 Degrees Celsius per second and greater.

31. (Previously Presented) The method of claim 29 wherein said first surface roughness value is reduced by at least about ninety percent to the second roughness value.

32. (Previously Presented) The method of claim 29 wherein said HCl gas and said hydrogen gas are a ratio ($HCl:H_2$) of about 0.001 to 30.

33. (Previously Presented) The method of claim 29, wherein said hydrogen gas and the HCl gas interact with said cleaved surface to reduce said surface roughness value.

34. (Previously Presented) The method of claim 29 wherein said first surface roughness value of said cleaved surface is reduced in a thermal processing chamber.

35. (Previously Presented) The method of claim 29 wherein cleaved surface is provided by a controlled cleavage process.

36. (Previously Presented) The method of claim 29 wherein said SOI substrate is fabricated from a donor silicon wafer.

37. (Previously Presented) The method of claim 29 wherein said surface is raised to a temperature of at least about 1,000° Celsius.

38. (Previously Presented) The method of claim 29 wherein said environment is a process chamber wherein said substrate is provided.

39. (Previously Presented) The method of claim 29 wherein the environment is maintained at a pressure of about 1 atmosphere.

40. (Previously Presented) The method of claim 29 wherein said SOI substrate is a wafer whereon a plurality of fabrication processes are performed to define a plurality of transistors on said substantially planarized surface.

41. (Previously Presented) The method of claim 29, wherein said SOI substrate is a wafer having a main surface, said main surface being planarized in its entirety by said increasing a temperature and contacting steps, wherein a plurality of devices are fabricated on said planarized main surface.

42. (Previously Presented) A dry method for finishing SOI wafers, said method comprising:

providing an SOI wafer comprising a main surface that has been cleaved, said cleaved main surface having a first surface roughness value;

performing a hydrogen treatment to increase a hydrogen concentration of said cleaved main surface; and

performing an etchant and thermal treatment after the hydrogen treatment, the etchant and thermal treatment comprising:

increasing a temperature of an environment associated with said cleaved main surface to greater than about 1,000° Celsius; and

contacting said cleaved main surface with a hydrogen bearing environment at least when said temperature of said environment is greater than about 1,000° Celsius to reduce said first surface roughness value by at least about eighty percent to a second surface roughness value, said hydrogen bearing environment including at least an HCl gas and a hydrogen gas;

wherein the main surface is substantially planarized in its entirety to the second roughness value, the planarized main surface providing a surface whereon a plurality of devices are later defined.

43. (Previously Presented) The method of claim 29 wherein the hydrogen treatment increases the concentration of hydrogen of said cleaved surface to a range of 10^{21} and 5 x 10^{22} atoms/cm^3.

44. (Previously Presented) The method of claim 29 wherein the hydrogen treatment comprises at least one of implantation, diffusion, or a combination of implantation and diffusion.

45. (Previously Presented) The method of claim 29 wherein said temperature of said environment is in the range of 1,000° Celsius and 1,200° Celsius.

10. EVIDENCE APPENDIX

Attached hereto is the DECLARATION OF SIEN G. KANG UNDER 37 CFR §1.132, originally filed May 1, 2006 in support of the RESPONSE ACCOMPANYING REQUEST FOR CONTINUED EXAMINATION also filed on that date.

11. RELATED PROCEEDINGS APPENDIX

None

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

On May 1, 2006

TOWNSEND and TOWNSEND and CREW LLP

By: Eleanor J. Taylor

PATENT
Attorney Docket No.: 018419-008320US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

SIEN G. KANG et al.

Application No.: 09/893,340

Filed: June 26, 2001

For: SURFACE FINISHING OF SOI SUBSTRATES USING AN EPI PROCESS

Customer No.: 20350

Confirmation No. 2640

Examiner: Jack S.J. Chen

Technology Center/Art Unit: 2813

DECLARATION OF SIEN G. KANG UNDER 37 CFR §1,132

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I declare as follows:

1. I am a co-inventor of the above-referenced patent application. I have extensive experience and education in the field of manufacturing semiconductor substrates. Based upon my training, I do not think one of ordinary skill in the art of manufacturing semiconductor substrates, would have been motivated to combine the prior art references relied upon by the

Examiner to reject the claims pending in the instant application. In particular, I do not believe that one of ordinary skill would have found suggestion to combine the Ohshima Patent and Moriceau Article references dealing with manufacture of substrates, with the Benton Patent dealing with the fabrication of devices in semiconducting chips. The basis for my conclusion is provided below.

2. My formal education is as a chemical engineer. In 1979 received my Bachelor of Science degree in Chemical Engineering at the University of Lowell in Lowell, Massachusetts. In 1983 I received a Master's degree in Chemical Engineering from Pennsylvania State University in University Park, Pennsylvania.

3. I have extensive experience working for Silicon Genesis Corporation ("SiGen") in the field of manufacturing semiconductor substrates. SiGen is a manufacturer of semiconductor substrates formed from multiple layers of material, for example silicon-on-insulator (SOI) substrates such as silicon-on-oxide, silicon-on-sapphire, and silicon-on-quartz. Examples of other types of multi-layer semiconductor substrates include silicon-on-germanium, and silicon-on-silicon. I am currently employed by SiGen as an Integration Manager, where my duties include overseeing the work of the engineers responsible for fabricating and testing the quality of different types of multilayer substrates. Prior to working as an Integration Manager, since 1998 I worked for SiGen first as a Project Engineer, and then as a Project Manager.

4. Prior to joining SiGen in 1998, I had over eleven years worth of experience in the semiconductor industry. For example, from 1996-1998, I was a Senior Member of the Technical Staff for the Institute of Microelectronics (IME) located in Singapore. In this position, my duties included preparing metallization tools for operation in a newly-constructed fabrication facility. For ten years prior to joining IME, from 1986-1996 I worked in various process engineering positions for Genus, Inc. of Sunnyvale, California, where my job duties included the design of tools for use in depositing tungsten-containing materials such as tungsten nitride and tungsten silicide. From 1984-1986, I was employed by Intel Corp. as a Process Engineer, where my

duties included line operation of a semiconductor device tool utilized in formation of layers of metallization in a memory device.

5. I have reviewed in detail the following materials relating to prosecution of the instant patent application:

a. Office Action including Final Rejection of Claims Mailed November 2, 2005, attached hereto as Exhibit A;

b. U.S. Patent 6,251,754 to Ohshima et al. ("the Ohshima Patent") relied upon by the Examiner in the Office Action of November 2, 2005 and attached hereto as Exhibit B;

c. U.S. Patent No. 5,141,878 to Benton et al. ("the Benton Patent") relied upon by the Examiner in the Office Action of November 2, 2005 and attached hereto as Exhibit C;

d. Moriceau et al., "Hydrogen annealing treatment used to obtain high quality SOI surfaces", IEEE Intl'l SOI Conference Proceedings 37-38 (1998) ("the Moriceau Article") relied upon by the Examiner in the Office Action of November 2, 2005 and attached hereto as Exhibit D;

I understand that the Examiner has rejected many of the pending claims of the instant application as obvious based upon the Ohshima Patent in combination with the Moriceau article and the Benton Patent.

6. Based upon my experience and training, I do not believe that one of ordinary skill in the art of manufacturing semiconductor substrates, would have been motivated to combine the reference teachings relied upon by the Examiner in order to devise the claimed invention. In particular, both the Ohshima Patent and the Moriceau Article specifically relate to the field of manufacturing semiconductor substrates. The Oshima Patent describes a method of manufacturing a semiconductor substrate, and the Moriceau Article describes a method of treating a surface of a substrate. By contrast, the Benton Patent relates to the field of fabricating active devices on semiconductor chips. In particular, the Benton Patent describes fabrication of a photodiode structure on a silicon substrate that has already been manufactured and provided. Because of the substantially different fields (i.e. substrate manufacture vs. chip fabrication)

implicated by the Ohshima Patent/Moriceau Article and the Benton Patent, I do not believe that one of skill in the art would have been motivated to combine these references.

I hereby declare that all statements made herein of my own knowledge are true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Sien G. Kang

4/27/06
Dated

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